IN THE CLAIMS

Please amend the claims as follows. This listing of claims will replace all prior

versions, and listings, of claims in the application.

1. (currently amended) An product suitable for simulating a standard wafer in

semiconductor manufacturing equipment, comprising:

a first layer composed of a material suitable for being handled by the

semiconductor manufacturing equipment; and

a second layer composed of a mixture of multiple materials disposed entirely

over the first layer, the mixture of the multiple materials configured to simultaneously

generate byproducts during an etching operation, wherein the byproducts are selected

from the group consisting of aluminum, silicon, tungsten, tungsten silicide, titanium,

titanium nitride, silicon dioxide, platinum, ruthenium, ruthenium oxide, copper,

tantalum, and nickel similar to byproducts produced by the standard wafer.

2. (previously presented) The product of claim 1, wherein the multiple materials

include a photoresist and a metal.

3. (previously presented) The product of claim 1, wherein the multiple materials

include both a polymer and a material selected from the group consisting of silicon, tungsten,

tungsten silicide, titanium, titanium nitride, silicon dioxide, aluminum, platinum, ruthenium,

ruthenium oxide, copper, tantalum, and nickel.

Claims 4-15 (canceled)

Amendment

2

Atty. Docket No. LAM2P267A

App. No. 09/923,725 Amendment dated July 30, 2004

Reply to Office Communication of July 26, 2004

16. (previously presented) The product of claim 1, wherein the mixture of multiple

materials includes three or more materials.

17. (previously presented) The product of claim 1, wherein the second layer is

capable of withstanding cumulative etching time of up to 120 radio frequency minutes.

18. (previously presented) The product of claim 1, wherein the mixture of the

multiple materials are baked on the first layer.

19. (previously presented) The apparatus of claim 1, wherein a ratio of the

multiple materials in the mixture corresponds to an exposed area on the standard wafer being

simulated.

Claims 20-39 (canceled)

Claims 40-58 (canceled)